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# Experimental Study on the Electrical Characteristic of a GaN Hybrid Drain-embedded Gate Injection Transistor (HD-GIT)

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**Abstract–The hybrid drain-embedded gate injection transistor (HD-GIT) is a well-developed structure of GaN-based power transistor which solves the issues of current collapse and negative gate threshold voltage. In this paper, the electrical characteristic of a HD-GIT-based GaN power transistor is investigated with experimental study. Based on the gate I-V relationship, the design of the gate driver circuit is discussed. The gate driving losses as well as the switching waveforms of the HD-GIT under hard-switching operations are analyzed. Besides speeding up the switching operation, the reduction in the gate voltage and gate charge saves the gate driving power. These features substantially increase the maximum operating frequency of the HD-GIT-based power converter. The current collapse free operation allows the device working at a wide range of voltage and duty cycle without notable degradation of the dynamic on-state resistance.**

**Keywords–Gallium Nitride (GaN), high-electron-mobility transistor (HEMT).**

## I. INTRODUCTION

Semiconductor switches are the key elements of power electronic converters. At present, these power semiconductor devices in the industry are mainly based on the mature Si technology. However, the increasing requirements of high-frequency and high-voltage capabilities of these devices are reaching the physical limits of the Si technology. In order to get rid of the bottleneck in the performance of switching devices, the semiconductor industries have started seeking for alternative power semiconductor materials in recent years. The wide bandgap (WBG) semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) exhibit many superior features over the conventional counterparts. These features include: high blocking voltage, high electron velocity as well as high-temperature capability [1-3], which make these WBG semiconductor materials highly potential for the future power devices.

The GaN-based high electron mobility transistors (HEMTs) have demonstrated remarkable improvements on the power density and efficiency for high frequency power applications such as radiofrequency (RF) and microwave amplifiers. [4-8] In recent years, the adoption of GaN transistors in power converter applications has been reported and confirmed the potential in small footprint and efficient DC-DC converters with conventional hard-switched topologies [9-10]; bidirectional converters for energy storage systems in DC microgrids [11]; integrated converters for vehicular applications [12]; as well as single-phase AC inverters for low-frequency power supply [13] and high-frequency wireless power transfer [14].

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Along with the GaN technology maturation, the GaN switches show prominent competitive power in the market. For example, the development of GaN-on-Si fabrication techniques [15-19] has noticeably reduced the material cost; the cascode structure [20] and the gate injection technology [16] offer the normally off options which make them more ready for direct substitution of the Si counterparts. Engineering samples of GaN power transistors are currently available in the market for research and development purposes. In this paper, the experimental study of the GaN power transistor sample with the latest hybrid drain-embedded gate injection transistor (HD-GIT) structure [21] is presented. The electrical characteristic of the HD-GIT sample was measured and modeled. Also, the design considerations such as the gate driver circuit and the switching loss analysis are discussed.

## II. REVIEW ON THE HD-GIT TECHNOLOGY

The HD-GIT structure [21-24] is an improved version of HEMT which also utilizes 2D electron gas with high electron mobility formed at the interface between GaN and AlGaN for conduction; but the gate threshold voltage is altered for normally-off operation [17], [24] and the current-collapse issue is eliminated [22-23].

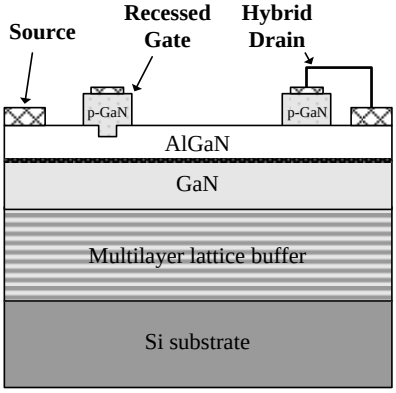



Fig. 1: Simplified schematic cross section diagram of the HD-GIT structure [21-23]

The simplified schematic cross section of the HD-GIT structure is illustrated in Fig. 1 [21-23]. The holes injected from the p-doped recessed gate significantly increase the threshold voltage of the transistor and make the GIT normally-off. When voltage is applied across the gate and the source which is exceeding the GIT's threshold voltage, the hole is injected to the channel and the electrons can flow with high mobility. Since the hole mobility is significantly lower than that of electrons, the gate current is kept at low level, in the order of mill-amperes. Besides, the supplementary p-GaN region adjacent to the drain electrode suppresses the current-collapse issue by injecting

holes which recombine with the trapped electrons near the channel [22-23].

For the consideration of material cost effectiveness, the GIT is grown on silicon substrate; the lattice and thermal mismatches [17], as well as the wetting issues [15] are avoided by insertion of the multilayer lattice buffer [21]. The designs in [17] and [22] suggest that the buffer could be formed by AlGaN/AlN and GaN/AlN layers.

## III. Specification of the HD-GIT Sample

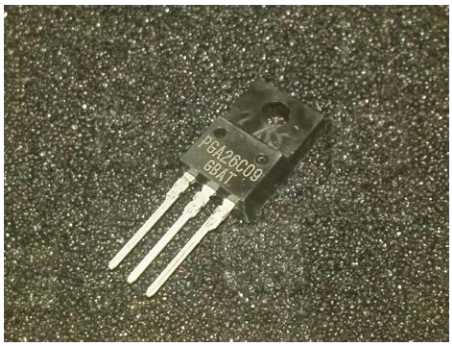



Fig. 2: The PGA26C09DV [25] HD-GIT sample in TO-220D package

**Table 1: Specification of the HD-GIT sample [25]**

| Item | Value |
|---|---|
| Package | TO-220D |
| $V_{ds(max)}$ | 600V |
| $I_{d(max)}$@$T_c$ = 25℃ | 15A |
| $R_{ds(on)}$ @$I_{gs}$ = 21.4mA and $T_j$ = 25℃ | 71mΩ |
| $V_{gs}$ | -10V to 4.5V |
| $V_{gs(th)}$ | 1.2V |
| $r_g$ | 4.4Ω |
| $Q_g$ @$V_d$ = 400V and $I_{ds}$ = 8A | 6nC |

In this work, the PGA26C09DV [25] X-GaN power transistor in TO-220D package (Fig. 2), was used to study the electrical characteristic of HD-GIT structure-based GaN power transistor. The voltage and current ratings are 600V and 15A, respectively. Referring to the preliminary datasheet [25] provided by the supplier, the basic specifications of the HD-GIT are listed in table 1.

## IV. Electrical Characteristic of the HD-GIT

The HD-GIT has different gate characteristic comparing to ordinary MOSFETs. Continuous gate current at mill-amperes is required to keep the device at on state. The $I_{gs}$-$V_{gs}$ characteristic can be simulated as a diode connecting between the gate and the source terminals. A simplified electrical model of a GaN HEMT is depicted in Fig. 3 [26-27]. At steady-state, the gate terminal is equivalent to a diode with series resistance. The drain is represented by a current source with gate voltage dependent transconductance $g_m$ and series resistances connecting to the source terminal.

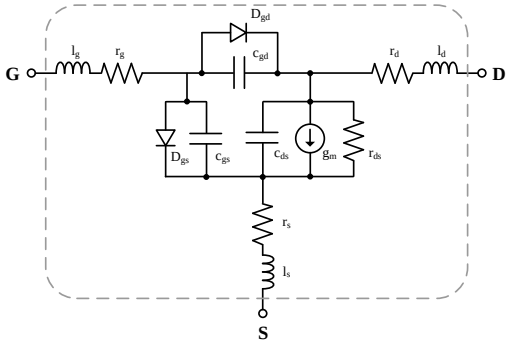



Fig. 3: Simplified electrical model of the GaN HEMT [26-27]

In order to examine the electrical characteristic of the device at steady-state, as well as during switching operation, the experimental setups with respective measuring circuits were implemented.

### *1. Gate Characteristic*

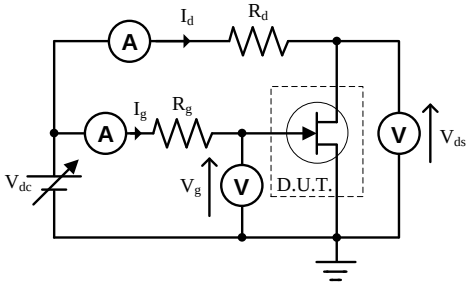



Fig. 4: The schematic of the experimental setup for measuring the steady-state gate characteristics of the HD-GIT

The measurement setup for steady-state gate characteristic is shown in Fig. 4. The external gate resistor, $R_g$, and drain resistor, $R_d$, were 1kΩ and 250Ω, respectively. By varying the voltage source, $V_{dc}$, the $I_{gs}$-$V_{gs}$ curve and the corresponding steady-state drain-to-source resistance were measured.

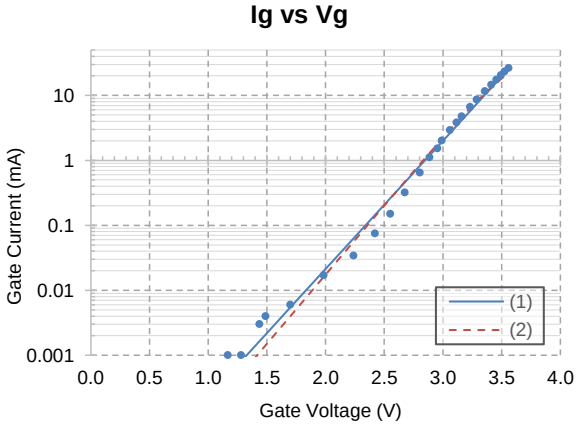
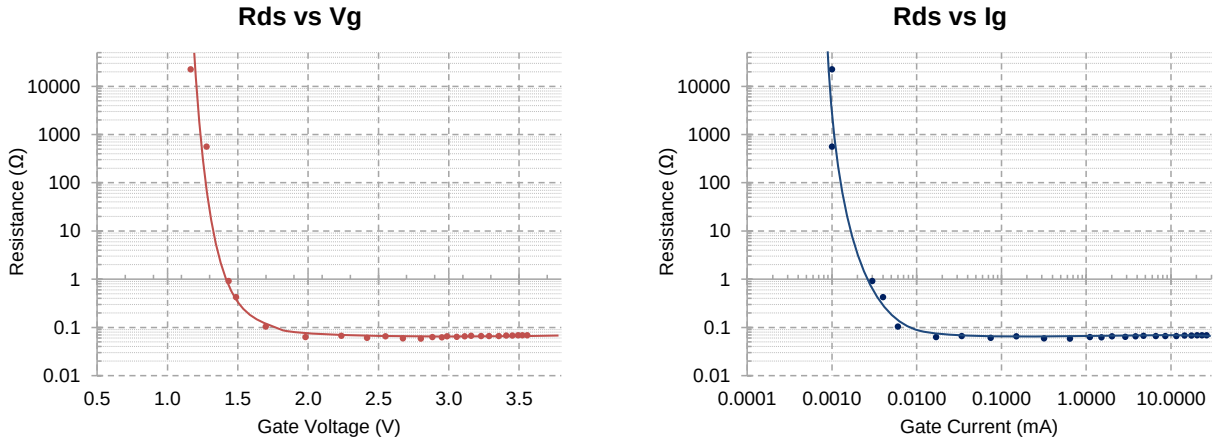



Fig. 5: The measured gate current to gate voltage ($I_{gs}$-$V_{gs}$) characteristic of the HD-GIT and the fitted curves ($T_a$ = 23℃)

The gate current to gate voltage ($I_{gs}$-$V_{gs}$) curve is plotted in Fig. 5. By directly fitting the measured data with the well-known diode equation, the gate current could be approximated by the following function.




(a) (b)

Fig. 6: Measured drain-to-source resistance $R_{ds}$ of the HD-GIT sample ($T_a$ = 23°C); (a) $R_{ds}$ to the gate voltage, $V_{gs}$; (b) $R_{ds}$ to the gate current, $I_{gs}$

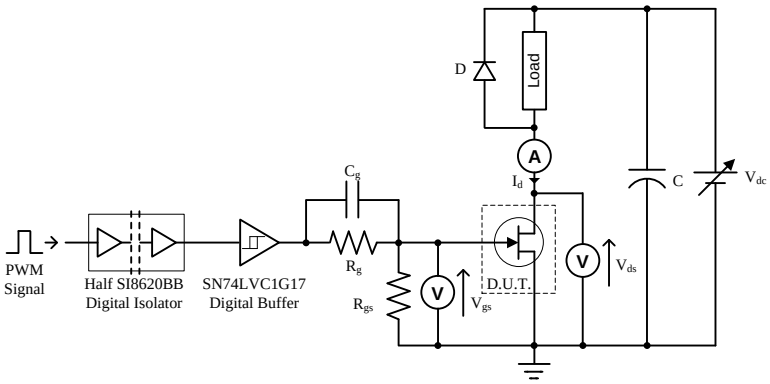



Fig. 7: The testing circuit, comprising an isolated gate driver and a loading circuit, for the low side HD-GIT

$$I_g = 2.4e-9\left(e^{\frac{V_{gs}}{0.22}}-1\right) \quad (1)$$

If the listed gate resistance, $r_g$ = *4.4Ω*, is used to adjust the measured gate voltage, the fitted equation becomes

$$I_g = 9.6e-10\left(e^{\frac{V_{gs}-4.4I_g}{0.204}}-1\right) \quad (2)$$

As shown in Fig. 5, it could be observed that the difference between the fitted curves, (1) and (2), is insignificant. In most cases, the simplified curve (1) would be accurate enough for the calculation of external gate resistor value, $R_g$ in power switching applications.

At the same time, the on-state drain-to-source resistance, $R_{ds}$, was measured with $V_{ds}$ and $I_{ds}$. The responses of $R_{ds}$ to the gate voltage and current are plotted in Fig. 6. The measured curve in Fig. 6(a) was similar to the $R_{ds}$ to gate voltage curves of logic level MOSFETs. The $R_{ds}$ of the HD-GIT dramatically dropped at the gate threshold voltage of around 1.2V and cropped at about 65mΩ. However, unlike the MOSFETs, the HD-GIT requires continuous gate current to hold the device at on state (Fig. 6(b)). At gate plateau voltage of around 1.5V, the gate current was about 5μA.

*2. Gate Driver Circuit*

Based on the measured gate characteristic of the HD-GIT in previous section, the drain-to-source resistance of the device reaches stable value at around $V_{gs}$ = 3V and $I_{gs}$ = 2mA. By adding a margin of 0.3V to 0.5V and substitute the gate-to-source voltage values into (1), the steady-state gate current, $I_{g(on)}$ would be about 7.84mA to 19.47mA. Considering that the gate driving losses are determined by the operating voltage of the gate driver; instead of ordinary gate driver of 10V to 15V operating voltage, a Schmitt-trigger buffer, SN74LVC1G17, which operates at 5V, was employed. The external gate resistance, $R_g$, was selected according to (3),

$$R_g = \frac{V_{OH} - V_{gs(on)}}{I_{g(on)}} \quad (3)$$

where $V_{OH}$ is the high-level output voltage of the digital buffer.

In order to speed up the on and off transients, a series connected capacitance, $C_g$, was added between the buffer's output and the gate terminals for providing inrush current to charge up the intrinsic capacitance quickly; and also providing negative voltage to ensure off state of the device during low output logic level of the buffer. The selection of $C_g$ follows equation (4) [28].

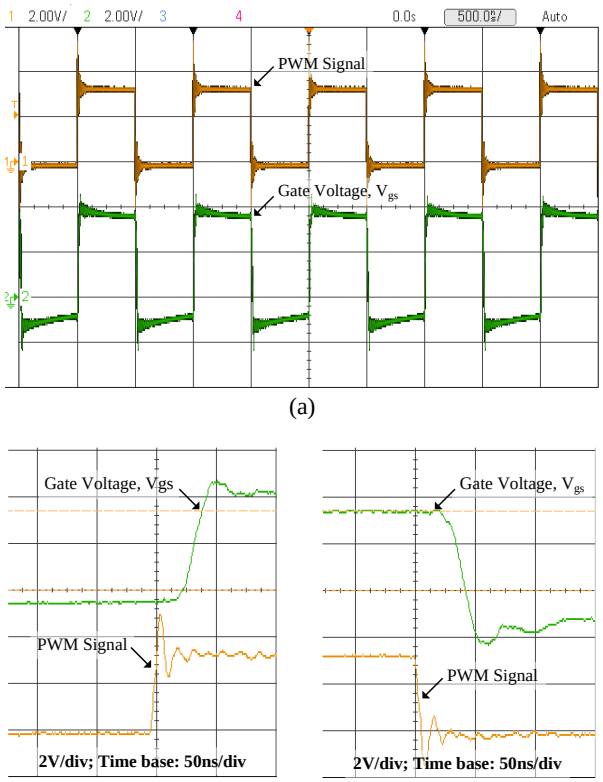



Fig. 8: The measured gate waveforms at 1MHz and 50% duty cycle; (a) the PWM signal and the corresponding gate voltage; (b) zoomed in waveforms at ON transient; (c) zoomed in waveforms at OFF transient

$$C_g = \frac{Q_g}{V_{OH} - V_{gs(on)} - V_{neg}} \tag{4}$$

In addition, an external parallel resistor, $R_{gs}$, with high resistance was inserted between the gate and source terminals of the device to pull the gate voltage down and ensure the device is in off state when the gate driver circuit is not powered. Based on the listed values in the datasheet of the HD-GIT and on-state voltage margin of 0.3V to 0.5V and negative voltage of 1V, the calculated $R_g$ and $C_g$ were 77.0Ω to 216.8Ω and 10.9nF, respectively.

In the testing circuit, external gate resistance of $R_g$ = 100Ω, and series capacitor of $C_g$ = 10nF were selected. Moreover, a low-power digital isolator, SI8620BB, was employed to provide galvanic isolation between the signal and power circuits. The gate driving waveforms at 1MHz, generated by the testing circuit, are shown in Fig. 8. The propagation delay time was around 32ns, while the rise and fall time were around 14ns for both turning on and off.

*3. Hard-switching Performance*

A voltage source of $V_{dc}$ = 50V and an inductive load of about 10Ω were employed in the testing circuit. The HD-GIT was switched at 500kHz. The drain-to-source voltage and the drain current waveforms of the device under hard-switching operation were measured (Fig. 9). As illustrated in the switching waveforms, the durations for the HD-GIT to turn on and off under loading were approximately 20ns and 12ns, respectively. In general, shorter durations for turning on and off would cause lesser switching losses in hard-switched power converters.

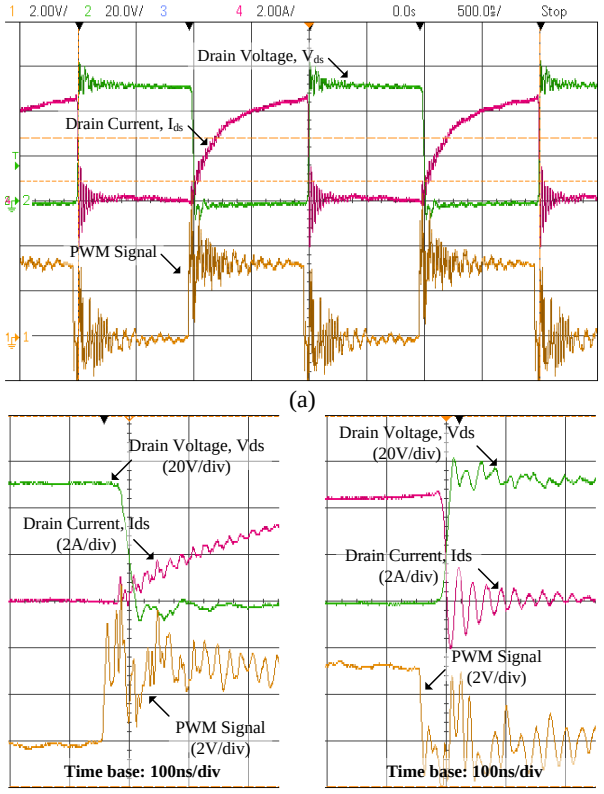



Fig. 9: The measured output waveforms at 500kHz and 50% duty cycle; (a) the PWM signal and the corresponding drain voltage and current; (b) zoomed in waveforms at ON transient; (c) zoomed in waveforms at OFF transient

### 3.1. Gate driving Loss Analysis

The gate driving losses for the HD-GIT consist of two major parts – 1) the charge-up losses of the device's intrinsic capacitance, and 2) the conductance losses caused by continuous gate current during on-state. Therefore, the gate driving losses, $P_{drive}$, would be approximately

$$P_{drive} = V_{OH}\left(DI_{g(on)} + fQ_g\right) \tag{5}$$

where D is the duty cycle and *f* is the switching frequency of the device. Although the HD-GIT requires continuous gate current at on state, the reduction in the driving voltage and gate charge could significantly reduce the gate driving losses at high frequency operation.

### 3.2. Switching Loss Analysis

The magnitude of the energy losses during the ON and OFF operations of the switches are highly dependent on the switching duration, $T_{sw}$, which the voltage and current waveforms of the switch are overlapping each other. The switching energy losses, $E_{sw}$, can be evaluated as (6).

$$E_{sw} = \int_0^{T_{sw}} V_{ds}(t)\, I_{ds}(t)\, dt \tag{6}$$

which can be estimated by linear approximation and simplified to

$$E_{sw} = \frac{V_{ds(off)} I_{ds(on)} T_{sw}}{6} \tag{7}$$

where $V_{ds(off)}$ is the drain-to-source voltage across the transistor before the on transition or after the off transition while $I_{ds(on)}$ is the drain current of the transistor before the off transition or after the on transition. Hence, the switching power losses, $P_{sw(loss)}$, of the semiconductor switches are directly proportional to the operation frequency and the duration of the switching operations.

$$P_{sw(loss)} = \frac{fT_{sw}V_{ds(off)}I_{ds(on)}}{3} \quad (8)$$

Considering the product, $V_{ds(off)}I_{ds(on)}$, is the order of power handling of the semiconductor switches, in order to keep the switching losses below the target factor, α, the maximum operation frequency, $f_{max}$, of the hard switching semiconductor switch should be

$$f_{\max} = \frac{3\alpha}{T_{sw}} \quad (9)$$

For example, if the target switching losses factor is 1%; and the WBG switch having average hard switching duration of 20ns, the maximum operation frequency would be

$$f_{\max} = \frac{3\times 0.01}{20e-9} = 1.5MHz \quad (10)$$

*5. Study on the Current Collapse Issue*

Current collapse due to trapping effects is characterized in conventional AlGaN/GaN HEMTs that the $R_{ds(on)}$ increases dramatically after applying voltage stress across the drain and source terminals of the device [29]. The degradation of dynamic on-state resistance [30] at high operating voltage would pose a challenge to power electronics design engineers. The HD-GIT structure employed in the sample device of this study was featured as current collapse free [25] at the rated voltage. This feature has been demonstrated in [22] and [23] by applying high voltage pulses with fixed duty cycle to analyze the saturated dynamic $R_{ds(on)}$.

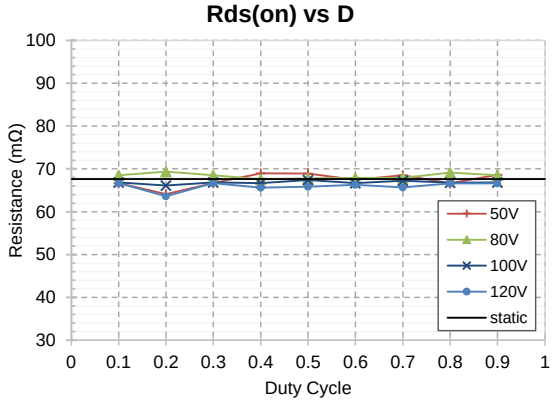



Fig. 10: The measured on-state resistance of the HD-GiT sample under different duty cycle, D, and applied voltage

As the trapping effects is a time-accumulative phenomenon [29-30], duty cycle was used as the variable to demonstrate the equilibrium $R_{ds(on)}$. As illustrated in Fig. 10, no distinct relationship between the on-state resistance and duty cycle could be observed, which suggests that the effects of the dynamic $R_{ds(on)}$ of this HD-GIT would be negligible in practical application.

## V. SUMMARY

The WBG semiconductor devices have exhibited their superiority features over the conventional Si technology. The HD-GIT is one of the most well developed structures for GaN power transistors which overcome many practical issues such as the unstable and negative gate threshold voltage and the current collapse phenomenon. Comparing with Si-based MOSFETs and IGBTs, the GaN HEMTs have quite different electrical characteristics; therefore, the gate driver design, hard-switching feature as well as the dynamic on-state resistance should be taken into consideration in the substitution of Si-based devices. This paper demonstrates the gate and switching characteristics of a HD-GIT in circuit design point of view. Due to the reduction in the gate charge and required gate voltage, the gate driving losses at high frequency operation could be greatly reduced compared to the Si-based MOSFETs and IGBTs. The substantial increase in switching speed and the current collapse free operation allow hard-switched power converter design at high power density.

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